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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	54

Application Number	09/733,104
Filing Date	12/7/2000
First Named Inventor	Steven Teig
Group Art Unit	2815
Examiner Name	Chu, Chris C.
Attorney Docket Number	SPLX.P0004

Enclosures (Check all that apply)

- [x] Fee Transmittal Form
  - [ ] Fee Attached
  - [x] Credit Card Payment Form
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declarations(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Documents
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Assignment Papers (for an application)
- [ ] Drawing(s) (* Sheets)
- [ ] Response to Restriction Requirement
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] After Allowance Communication to Group
- [x] Appeal Communication to Board of Appeals and Interferences (**Appeal Brief in triplicate**)
- [ ] Appeal Communication to Group
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosures (*Listed below*): **Postcard**

Remarks:

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *Or* Individual name	Jeffrey A. McKinney, Reg. No. 43,795 of Stattler Johansen & Adeli LLP
Signature	
Date	June 3, 2003

CERTIFICATE OF MAILING

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Typed r printed nam	Jeffrey A. McKinney		
Signature		**Date**	June 3, 2003

FEE TRANSMITTAL FORM

TOTAL AMOUNT OF PAYMENT	$320.00

Complete if Known	
Application Numb r	09/733,104
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METHOD OF PAYMENT (check one)

☐ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:
Deposit Account Number: **50-1128**
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Stattler, Johansen & Adeli, LLP
☒ Charge Any Additional Fee Required Under 37 CFR §§ 1.16 and 1.17

☒ Payment Enclosed:
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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	
				SUBTOTAL (1)	

2. EXTRA CLAIM FEES

			Extra Claims	Fee from below	Fee Paid
Total Claims:		- 20 =		× 18 =	
Independent Claims:		- 3 =		× 80 =	
Multiple Dependent:				270 =	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple depend. claim, if not paid
109	80	209	40	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Code	Large Entity Fee	Small Entity Code	Small Entity Fee	Fee Description	Fee Paid
105	130	205	65	Surchg – late filing fee or oath (Missing Parts)	
127	50	227	25	Surchg – late prov. filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Reqest. pub. of SIR prior to Examiner action	
113	1,840*	113	1,840*	Req. publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	$320
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive – unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt.	
581	40	581	40	Recordation (Assignment) Fee (X ea. prop.)	
146	710	246	355	Filing submission aft final rej.(37CFR §1.129(a))	
179	710	279	355	Request for Continued Examination (RCE)	
				SUBTOTAL (3)	$320.00

Name	Jeffrey A. McKinney	Registration No. (Attorney/Agent)	43,795	Telephone	(650)752-0990 ext. 103
Signature				Date	June 3, 2003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

#15 Appeal Brief J McCarville 6/11/03

In re Patent Application for:

Steven Teig

Serial No.: 09/733,104

Filing Date: 12/07/2000

For: MULTI-DIRECTIONAL WIRING ON A SINGLE METAL LAYER

Examiner: Chu, Chris C.

Group Art Unit: 2815

APPEAL BRIEF

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Appeal from the final rejection of claims 1-17 in the above-referenced application. In accordance with 37 C.F.R. § 1.192, this Brief, along with the accompanying Appendices, is filed in triplicate and is accompanied by the required fee. Please charge any additional fees or credit any overpayment to Deposit Account No. 501128.

I. REAL PARTY IN INTEREST

The real party in interest to this Appeal is Cadence Design Systems, a Delaware Corporation, having its principal place of business in San Jose, California.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignees thereof.

III. STATUS OF CLAIMS

Claims 1-17 are pending in the present application. The examiner has rejected claims 1-17. Applicant hereby appeals the rejection of claims 1-17.

IV. STATUS OF AMENDMENTS

No amendments to the application were submitted after final rejection.

V. SUMMARY OF INVENTION

The claims (claims 1-16 and 17) are directed towards an integrated circuit having at least one metal layer that includes conductors to provide interconnectivity for the integrated circuit chip. For purposes of assigning preferred wiring directions for the conductors, the metal layer is divided into at least two sections (e.g., first section and second section). *Specification, page 2, lines 15-16.* Each section contains at least one thousand wires (*i.e.*, conductors) to interconnect points on the integrated circuit. *Specification, page 2, lines 16-17.* The conductors in each section are oriented in a preferred direction relative to the boundaries of the integrated circuit chip. A "preferred direction" is a direction in which at least fifty percent of the conductors are oriented. *Specification, page 2, lines 17-20.* **Figure 10** illustrates an example metal layer with multiple preferred directions.

The first and second sections of the claimed integrated circuit have different preferred wiring directions. One of the sections has a preferred wiring direction that is diagonal. A diagonal direction is neither vertical nor horizontal. Examples of diagonal directions include octalinear (*i.e.*, plus or minus 45 degrees from vertical or horizontal) and hexalinear (*i.e.*, plus or minus 30 or 60 degrees from vertical or horizontal). *Specification, page 3, lines 4-8; see also, page 6, lines 12-16.* **Figure 1b** illustrates an example of an integrated circuit that employs diagonal wiring. Furthermore, one of

the sections contains at least one conductor deposed in a Manhattan direction coupled to a conductor deposed in a diagonal wiring direction. *See, for example,* ***Figure 14***. A "Manhattan direction" is either vertical or horizontal. *Specification, page 3, lines 4-6.* **Figure 6a** illustrates an embodiment for a legacy Manhattan metal layer configuration.

VI. ISSUES

I. Whether the subject claims are unpatentable under 35 U.S.C. 112, first paragraph, as containing subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

II. Whether the drawings of the application disclosed every feature of the invention specified in the claims under 37 CFR 1.83(a).

III. Whether the subject claims are unpatentable under 35 U.S.C. 103(a) over Juengling (U.S. Pat. No. 6,448,591).

VII. GROUPING OF THE CLAIMS

Applicants contend that all of the pending claims (1-17) stand or fall together. Accordingly, applicants are not grouping the claims on appeal.

VIII. ARGUMENT

The examiner erred in rejecting the claimed invention by misapplying standards under 35 U.S.C. 112, first paragraph and 35 U.S.C. 103(a).

A. The Subject Claims Are Patentable Under 35 U.S.C. 112, First Paragraph.

In rejecting the subject claims under 35 U.S.C. 112, first paragraph, the examiner stated the following:

> Applicant does not specifically define in the rejected claims that the Manhattan or Manhattan wiring direction is a horizontal line direction. Also, applicant should notes [sic] that the usual meaning of the term "Manhattan" is a rectangular or right-angle rectilinear. Since Fig. 10 and Fig. 14 do not show the rectangular or right-angle rectilinear line coupled to a conductor deposed in the preferred wiring direction, the objection to the drawings and the 112 1st rejection are maintained. Further, applicant should notes [sic] that the features upon which applicant relies (i.e., horizontal line to read as the Manhattan direction) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. *Advisory Action mailed April 17, 2003.*

This statement raises at least three distinct issues: 1) How are applicants using the term "Manhattan direction" in the subject claims? 2) Do Figures 10 and 14 accordingly show a conductor deposed in a Manhattan direction as defined by applicants coupled to a conductor deposed in the preferred wiring direction? 3) Do applicants have to recite the meaning of "Manhattan direction" in the claims, where it has been defined in the specification?

1. Applicants' Use of the Term "Manhattan Direction" Is Clear.

Through description in the specification or presentation in figures, applicants have clearly defined the term "Manhattan direction" to mean either a horizontal direction or a vertical direction. On page 3, lines 4-6 of the application as filed, applicants state: "In one embodiment, the first preferred direction is a Manhattan direction (*e.g.*, horizontal or vertical), and the second preferred direction is a diagonal direction." Applicants further refer to wiring directions depicted in **Figures 6a-6d** as "Manhattan wiring." The only wiring directions shown in the figures are horizontal and

vertical, and these directions are labeled as such.

It is well-established law that an applicant may be his or her own lexicographer as long as any special meaning assigned to a term is "sufficiently clear in the specification that any departure from common usage would be so understood by a person of experience in the field of the invention." *MPEP 2111.01*, citing *Multiform Desiccants Inc. v. Medzam Ltd.*, 133 F.3d 1473 (Fed. Cir. 1998). Applicants have provided sufficient clarity in the specification such that one of ordinary skill would readily understand "Manhattan direction" to mean either "horizontal" or "vertical."

2. Figures 10 and 14 Show a Conductor Deposed in a Manhattan Direction.

Figures 10 and **14** depict wiring deposed in diagonal, horizontal and vertical directions. Since "Manhattan direction" is clearly and properly defined in applicants' specification to mean "horizontal" or "vertical," the subject figures show a conductor deposed in a Manhattan direction.

3. Applicants Do Not Have to Recite "Horizontal" and/or "Vertical" in the Claims Instead of "Manhattan Direction" to Comply With 35 U.S.C. 112, First Paragraph.

Importing limitations into a claim from the specification is typically improper. The issue with respect to this appeal, however, is not that principle; it is rather the definition of "importing." In this case, "importing" refers to the inclusion of a claim limitation that did not previously exist.

This difficult to understand concept is best seen through example. Take the example where a claim refers to "a hook," and another part of the patent specification states the following about term "hook":

> A hook is a curved device for catching, holding, or pulling. A hook may be made of steel, iron, plastic or other suitable material. Typically, a hook contains a barb.

Preferably, a hook is at least 2 inches long.

When reading the claim reciting "a hook," one would understand that "hook" refers to a "curved device for catching, holding, or pulling." One would not understand, however, that the hook was steel, contained a barb, and was at least 2 inches long. It is accordingly improper to read the "steel," "barb," or "length" limitations regarding the hook into the claim.

To paraphrase the above-presented example, one does not improperly import limitations into a claim where one simply reads a term to have its unambiguous meaning. A meaning is unambiguous where it only contains those elements of a term definition that cannot vary. For the example above, a hook is always a "curved device for catching, holding, or pulling." However, the composition of the hook (*e.g.*, steel), whether it contains a barb, and the length of a hook are all variable properties.

Applicants unambiguously defined "Manhattan direction" in their specification to mean "horizontal or vertical." That definition is invariable. It is accordingly proper to read "Manhattan direction" in the subject claims as "horizontal or vertical," and such a reading does not import limitations from the specification.

B. The Drawings of the Application Disclose the Features of the Invention Specified in the Claims Under 37 CFR 1.83(a).

In objecting to the drawings under 37 CFR 1.83(a), the examiner stated the following:

> The drawings must show every feature of the invention specified in the claims. Therefore, the following phrases "the second section further comprising at least one conductor deposed in a Manhattan direction coupled to a conductor deposed in said preferred diagonal wiring direction" and "the first section further comprising at least one conductor deposed in a diagonal direction coupled to a conductor deposed in the

Manhattan wiring direction" must be shown or the feature(s) canceled from the claim(s). *Final Office Action mailed September 26, 2002, page 2.*

1. Figures 10 and 14 Show Conductors Deposed in a Manhattan Direction Coupled to a Conductor Deposed in a Diagonal Direction.

As described above, **Figures 10** and **14** depict wiring deposed in a Manhattan direction, which applicant has defined as a horizontal or vertical direction. In **Figure 10**, wire 1042 is deposed in a Manhattan direction (*i.e.*, horizontal), and it is coupled to a conductor deposed in a preferred, diagonal (*i.e.*, hexalinear direction of plus 60 degrees) direction. *See also description on page 21 of the application, lines 3-4.* In Figure 14, wire 1410 is deposed in a Manhattan direction (*i.e.*, horizontal), and it is coupled to a conductor deposed in diagonal (*i.e.*, 45 degree) direction. *See also description on page 26 of the application, lines 3-4.* The drawings accordingly do show all the features of the claimed invention.

C. The Subject Claims Are Patentable Under 35 U.S.C. 103(a) over Juengling (U.S. Pat. No. 6,448,591).

In rejecting the subject claims under 35 U.S.C. 112, first paragraph, the examiner stated the following:

> Juengling does not disclose at least one thousand conductors situated in a contiguous area. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to adding at least one thousand conductors in a contiguous area, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). The ordinary artisan would have been motivated to modify Juengling in the manner described for at least the purpose of increasing the speed of the package. *Office Action mailed September 26, 2002, page 5.*

1. Juengling is Directed to Metallization Line Layouts that Avoid the Creation of Metallization Line Thinning and/or Disappearance for Excess Reflectance-Vulnerable Metallization Line Features.

Juengling delineates three significant problems for the process engineer seeking to fabricate metallization lines: 1) the focus offset sensitivity or depth of field capability of existing photolithographic equipment [col. 2, lns 65-67]; 2) lateral line thinning resulting from excess reflectance problems caused by photolithographic light [col. 3, lns 14-19]; and, 3) the possibility that interstitial particulate occurrence or a fabrication error will cause a bridge to form between adjacent metallization lines [col. 4, lns 18-22]. Juengling then proposes a way to address the problems. Specifically, he states that this objective is accomplished by "taking an existing metallization line layout that has been dictated by the fabrication of a semiconductor device array and . . . eliminating distant closest features that would otherwise cause the aforementioned problems . . . . " [Col. 4, lns 36-41]

The elimination of problematic distant closest features, according to Juengling, can be solved through at least four different means: 1) enhancing terminal ends of isolated metallization lines; 2) thickening metallization line widths to achieve substantially only nearby closest features; 3) filling spaces between metallization line features to achieve substantially standard preferred distance between any given metallization line feature and its nearest closest metallization line feature; and, 4) staggering unavoidable exposures to only have a single occurrence thereof on one side of the metallization line. [Col. 4, lns 41-55]

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/
/

2. Juengling's Figure 8 Illustrates the Enlargement and Enhancement of Metallization Lines on a Theoretical Layout Containing Less than Twelve Non 90-Degree Wires.

Juengling presented his Figure 8 simply to make the point that metallization lines with non 90-degree features could be enhanced and enlarged just as "Manhattan-style" lines could. [Col. 14, lns 20-23] The figure shows 11-diagonally directed metallization lines connected to 9 different horizontal lines. Several of the lines are shown to be enhanced or enlarged, including, for example, portions 876 and 711.

Juengling does not state that the diagonally directed metallization lines provide any advantage with respect to line processing. He does not point to any desirable quality at all for diagonally directed lines.

3. Applicants' Claims are Directed to an Integrated Circuit Containing at Least One Section Having at Least 500 Wires Flowing in the Same Diagonal Direction.

Applicants' independent claims 1 and 17 are directed to an integrated circuit, where each section of the integrated circuit comprises at least one thousand conductors. Furthermore, in at least one of the sections, at least fifty percent (*i.e.*, at least 500) of the conductors are oriented in the same diagonal direction:

> "[E]ach section comprising at least one thousand conductors situated in a contiguous area to interconnect points on the integrated circuit. . . ." *Claim 1, clause 1; and, Claim 17, clause 1.*
>
> "[W]herein a preferred direction, within a section, defines a direction, relative to the boundaries of the integrated circuit, for at least fifty percent of conductors in the section. . . ." *Claim 1, clause 1; and, Claim 17, clause 1.*
>
> "[A] second section comprising a preferred diagonal wiring direction for the conductors deposed in the second section." *Claim 1, clause 3; claim 17, clause 3.*

4. The Examiner Has Misapplied *In Re Boesch* to the Facts at Hand.

As presented above, in the September 26, 2002 Office Action, the examinar stated and/or implied that one of ordinary skill in the art viewing **Figure 8** of Juengling would have been motivated to modify Juengling's disclosure to arrive at Applicants' invention. To support his argument, the examiner stated that "optimizing" Juengling's **Figure 8** to arrive at an integrated circuit containing at least one section having at least 500 diagonal wires was routine. *Office Action, page 5.* He further cited *In re Boesch* as standing for that proposition.

In re Boesch is inapplicable to the facts at hand. It concerns the patentability of optimized "result-effective variables." "Result effective variables" are variables that achieve a recognized result. *MPEP 2144.05.* Specifically, if it is recognized that a variable controls a desirable result, then the optimum value for that variable is unpatentable under 35 U.S.C. 103; however, if one of ordinary skill would not understand that the variable is a result effective variable, then the optimum value for that variable could be patentable under 35 U.S.C. 103.

Juengling, in the case at hand, does not state that the number of diagonal wires affects any result. Certainly by increasing the number of diagonal wires, Juengling's method of enlarging and enhancing metallization lines would not be facilitated. Juengling, then, does not indicate that the number of diagonal wires is a result effective variable in integrated circuit design, and no one viewing Juengling would come to that conclusion. Applicants' invention is accordingly not an optimization of Juengling's.

5. The Examiner Has Improperly Used Applicants' Own Disclosure to Demonstrate a Motivation to Modify Juengling.

"The teaching or suggestion to make the claimed combination and the reasonable

expectation of success must both be found in the prior art, not in applicant's disclosure." *MPEP 2143.* In making his rejection under 35 U.S.C. 103(a) in view of Juengling, the examiner stated: "The ordinary artisan would have been motivated to modify Juengling in the manner described above [adding at least one thousand conductors] for at least the purpose of increasing speed of the package." *Office Action dated September 26, 2002, page 5.* Juengling, however, neither states nor suggests that adding at least one thousand conductors to his theoretical representation (*i.e.*, his **Figure 8**) would increase the speed of the package. His invention does not directly relate to package speed.

In contrast to Juengling, applicants explicitly point to their objective of increasing the operational speed of an integrated circuit:

> The distance of the wiring on the metal layers determines the propagation delay exhibited during operation of the circuit components. In turn, the propagation delay introduced in a circuit directly impacts the operational speed of the circuit). The length of the wire determines the amount of propagation delay introduced into a circuit (i.e., the longer the wire the greater the propagation delay). In addition, when circuit connections are routed between metal layers, using mechanisms referred to as "vias", a significant amount of additional propagation delay is introduced. Accordingly, it is desirable to reduce the length of wires necessary to interconnect electronic components in an IC to reduce the propagation delay and to enhance the operational speed of the IC. It is also desirable to minimize the number of circuit connections routed between metal layers to further reduce the propagation delay. *Specification, page 2, lines 1-11.*

Applicants further note that one way to achieve their objective is through the presently claimed invention. *See specification pages 2, line 14 to page 4, line 8.* Therefore, applicants' disclosure teaches that one can increase the speed of an integrated circuit by having a circuit section that contains at least 500 diagonal lines running in the same direction.

It is difficult to forget applicants' teachings while viewing art that the examiner believes is relevant to the patentability of applicants' invention, but that is the requirement under 35

U.S.C. 103. In this case, the requirement has not been met.

IX. CONCLUSION.

In view of the foregoing, applicants respectfully submit that the claims are patentable and the drawings fully comply with the appropriate rules. Applicants hereby request that the Board overturn the examiner's finding that the claims are unpatentable under 35 U.S.C. 112, first paragraph and 35 U.S.C. 103(a).

BY: _____
Jeffrey A. McKinney
Reg. No. 43,795
Date: June 3, 2003
Tel. No.: 650.752.0990 ext. 103

APPENDIX

The following claims are the subject of this Appeal.

1. An integrated circuit comprising:

at least one metal layer comprising a plurality of sections, each section comprising at least one thousand conductors situated in a contiguous area to interconnect points on the integrated circuit, wherein a preferred direction, within a section, defines a direction, relative to the boundaries of the integrated circuit, for at least fifty percent of conductors in the section;

a first section comprising a first preferred direction for the conductors deposed in the first section; and

a second section comprising a preferred diagonal wiring direction for the conductors deposed in the second section, such that the diagonal wiring preferred direction is a direction different from the first preferred direction, said second section further comprising at least one conductor deposed in a Manhattan direction coupled to a conductor deposed in said preferred diagonal wiring direction.

2. The integrated circuit as set forth in claim 1, wherein the first preferred direction comprises a diagonal direction.

3. The integrated circuit as set forth in claim 2, wherein the first preferred diagonal direction comprises a direction perpendicular to said preferred diagonal wiring direction in said second section.

4. The integrated circuit as set forth in claim 1, wherein the diagonal direction comprises an octalinear direction.

5. The integrated circuit as set forth in claim 1, wherein the diagonal direction comprises a hexalinear direction.

6. The integrated circuit as set forth in claim 1, wherein:

the first preferred direction comprises a first diagonal direction; and

the second preferred direction comprises a second diagonal direction, different from the first diagonal direction.

7. The integrated circuit as set forth in claim 6, wherein:

the first diagonal direction comprises an octalinear direction; and

the second diagonal direction comprises an octalinear direction complementary to the first diagonal direction.

8. The integrated circuit as set forth in claim 6, wherein:

the first diagonal direction comprises a hexalinear direction; and

the second diagonal direction comprises a hexalinear direction complementary to the first diagonal direction.

9. The integrated circuit as set forth in claim 6, wherein:

The first diagonal direction comprises an octalinear direction; and

The second diagonal direction comprises a hexalinear direction.

10. The integrated circuit as set forth in claim 1, further comprising at least one more additional section having a preferred direction comprising a diagonal direction.

11. The integrated circuit as set forth in claim 1, further comprising at least one more section having a preferred direction comprising a Manhattan direction.

12. The integrated circuit as set forth in claim 1, further comprising at least one additional wire deposed in a section with a direction different than the preferred direction of the section.

13. The integrated circuit as set forth in claim 12, wherein:

the preferred direction comprises a diagonal direction; and

the direction different than the preferred direction comprises a Manhattan direction.

14. The integrated circuit as set forth in claim 13, wherein:

the preferred direction comprises a diagonal direction; and

the direction different than the preferred direction comprises a Manhattan direction.

15. The integrated circuit as set forth in claim 13, wherein:

the preferred direction comprises a Manhattan direction; and

the direction different from the preferred direction comprises a diagonal direction.

16. The integrated circuit as set forth in claim 13, wherein the direction different than the preferred direction comprises a direction complementary to the preferred direction.

17. An integrated circuit comprising:

at least one metal layer comprising a plurality of sections, each section comprising at least one thousand conductors situated in a contiguous area to interconnect points on the integrated circuit, wherein a preferred direction, within a section, defines a direction, relative to the boundaries of the integrated circuit, for at least fifty percent of conductors in the section;

a first section comprising a Manhattan wiring direction for the conductors deposed in the

first section, the first section further comprising at least one conductor deposed in a diagonal direction coupled to a conductor deposed in the Manhattan wiring direction; and

a second section comprising a preferred diagonal wiring direction for the conductors deposed in the second section, such that the diagonal wiring preferred direction is a direction different from the first preferred direction.